NORTHWESTERN POLYTECHNIC

DEPARTMENT OF SCIENCE

COURSE OUTLINE –Winter 2023

CS3290 (A3): COMPUTER ORGANIZATION AND ARCHITECTURE II – 3 (3-0-3)
90 Hours for 15 Weeks

Northwestern Polytechnic acknowledges that our campuses are located on Treaty 8 territory, the ancestral and present-day home to many diverse First Nations, Metis, and Inuit people. We are grateful to work, live and learn on the traditional territory of Duncan's First Nation, Horse Lake First Nation and Sturgeon Lake Cree Nation, who are the original caretakers of this land.

We acknowledge the history of this land and we are thankful for the opportunity to walk together in friendship, where we will encourage and promote positive change for present and future generations.

INSTRUCTOR:	**Mohammad Mahdi Hassan**	**PHONE:**	
OFFICE:		**E-MAIL:**	
OFFICE HOURS:	TBA		

CALENDAR DESCRIPTION: This course is designed to provide an overview of logic design, number systems, digital circuits, combinational systems, memory, register transfer, control logic design, CPU design, and advanced topics on micro-computer architectures.

PREREQUISITE(S)/COREQUISITE: CS2290

REQUIRED TEXT/RESOURCE MATERIALS:
Logic and Computer Design Fundamentals 5th edition
Morris Mano, Charles Kime, Tom Martin
Pearson Education

DELIVERY MODE(S): In class lecture

COURSE OBJECTIVES:
Students will be introduced to digital computer architecture and its underlying digital logic including topics such as:

- Integrated circuits from basic logic gates to more complex chips (registers and ALUs)
- Fundamentals of digital logic analysis and design.

- Boolean Algebra and its relation to circuit design and minimization
- Combinational (no memory component) and sequential (memory) logic
- Single bit memory to more organized memory such as registers.
- Data paths, control unit design and generic CPU design.

LEARNING OUTCOMES:
Students will be able to:

- Understand and manipulate Boolean logic
- Design and build combinational circuits to perform a variety of tasks
- Design and build sequential circuits to perform a variety of tasks
- Reduce both sequential and combinational circuits
- Build a simple CPU which will include registers, ALU, data path and all the necessary circuitry required to decode and execute program code presented in a binary format.

TRANSFERABILITY:

Please consult the Alberta Transfer Guide for more information. You may check to ensure the transferability of this course at the Alberta Transfer Guide main page http://www.transferalberta.ca.

** Grade of D or D+ may not be acceptable for transfer to other post-secondary institutions. **Students are cautioned that it is their responsibility to contact the receiving institutions to ensure transferability**

EVALUATIONS:

30% -- Lab/Homework Assignments
10% -- Class Quizzes
25% -- Midterm
35% -- Final Exam

GRADING CRITERIA: (The following criteria may be changed to suite the particular course/instructor)

Please note that most universities will not accept your course for transfer credit **IF** your grade is **less than C-**.

Alpha Grade	4-point Equivalent	Percentage Guidelines		Alpha Grade	4-point Equivalent	Percentage Guidelines
A+	4.0	90-100		C+	2.3	67-69
A	4.0	85-89		C	2.0	63-66
A-	3.7	80-84		C-	1.7	60-62
B+	3.3	77-79		D+	1.3	55-59
B	3.0	73-76		D	1.0	50-54
B-	2.7	70-72		F	0.0	00-49

COURSE SCHEDULE/TENTATIVE TIMELINE:

Topic	Week
Boolean Algebra (basic identities, algebraic manipulation)	1
Logic gates	
Canonical Forms (minterms, maxterms, SOP, POS)	2
Applications of Boolean Algebra	
Karnaugh Maps (2,3,4,5 variable maps, implicants prime/essential, covering set)	3
Quine-McCluskey Method	4
Decoders/Encoders/Priority Encoders (decoder expansion)	5
Multiplexers/Demultiplexer (use of MUX in Boolean Function Implementation)	6
Latches/Flip-Flops (S-R, D, J-K, Master-Slave, Edge triggered)	7
Sequential Circuits (Characteristic/Excitation Tables, state diagrams, analysis and design)	8
Mealy/Moore Machines,	9
State Minimization	10
Counters (Ripple, Synchronous, Asynchronous, arbitrary, ring)	11
Registers (Shift, Bidirectional shift, Parallel load)	12
RAM (Static, Dynamic, RAM cells, address decoding, read/write, bit slice model)	13
PLDs (ROM, PROM, PLA, PAL)	14
VHDL	
Register transfers and Data Paths (registers, buses, ALU, micro-operations,)	15

STUDENT RESPONSIBILITIES:

- The Student must pass the theory/concepts portion of the course in order to obtain a passing grade for the term. In other words, a student must obtain 35 out of a possible 70 exam based marks - which includes all components except the lab assignments.
- LAB attendance is mandatory. You must clear all absences with me; failure to comply will result in a failing grade for the course!

STATEMENT ON PLAGIARISM AND CHEATING:

Cheating and plagiarism will not be tolerated and there will be penalties. For a more precise definition of plagiarism and its consequences, refer to the Student Conduct section of the Northwestern Polytechnic Calendar at https://www.nwpolytech.ca/programs/calendar/ or the Student Rights and Responsibilities policy which can be found at https://www.nwpolytech.ca/about/administration/policies/index.html.

**Note: all Academic and Administrative policies are available on the same page.