DEPARTMENT OF Science.

CS3290 –Computer Organization and Architecture II

Winter 2011

INSTRUCTOR: Libero Ficocelli **PHONE:** 780 539-2825

OFFICE: C424 **E-MAIL:** Libero@GPRC.ab.ca

OFFICE HOURS: By appointment

PREREQUISITE(S)/COREQUISITE: CS2290

REQUIRED TEXT/RESOURCE MATERIALS:

Theory: Digital Electronics with VHDL – Quartus II Version
Willian Kleitz

Lab: Rapid Prototyping of Digital Systems: A tutorial Approach
Second Edition
James Hamblen and Michael Furman
Copies will be made available in the lab

DESCRIPTION:

This course will introduce students to the fundamentals of logic design and computer architecture. Important topics will include (but not limited to) basic logic gates and circuits, circuit minimization, combinational logic, sequential logic, latches and flip-flops, registers and register transfers, ALU design, Control unit design, CPU design, I/O operations.

The lectures will stress the theoretical aspects of the material while the labs will deal with actual design and physical construction of digital circuits: we will be using a variety of LSI, MSI, EPROMs, and static rams chips in our circuit construction. We will also be making use of Quartus II software and the Altera UP2 Development kit to implement VHDL programming tasks.

CREDIT/CONTACT HOURS: 3 Credits – Lectures 3 Hrs; Lab 3 Hrs.

DELIVERY MODE(S): Lectures and Labs

TRANSFERABILITY: U of Alberta; U of Lethbridge; U of Calgary; Athabasca University; King's University College;

GRADING CRITERIA:

Homework Assignments / Lab Assignments/ Lab Reports	30%
Class Quizzes	10%
Midterm	25%
Final Exam	35%

TENTATIVE TOPICS:

- Boolean Algebra (basic identities, algebraic manipulation)
- Logic gates
- Cannonical Forms (minterms, maxterms, SOP, POS)
- Applications of Boolean Algebra
- Karnaugh Maps (2,3,4,5 variable maps, implicants prime/essential, covering set)
- Quine-McCluskey Method
- Multiple Output Networks (analysis and design)
- Decoders/Encoders/Priority Encoders (decoder expansion)
- Multiplexers/Demultiplexer (use of MUX in Boolean Function Implementation)
- Latches/Flip-Flops (S-R, D, J-K, Master-Slave, Edge triggered)
- Sequential Circuits (Charactersistic/Excitation Tables, state diagrams, analysis and design)
- Mealy/Moore Machines,
- State Minimization
- Counters (Ripple, Synchronous, Asynchronous, arbitrary, ring)
- Registers (Shift, Bidirectional shift, Parallel load)
- RAM (Static, Dynamic, RAM cells, address decoding, read/write, bit slice model)
- PLDs (ROM, PROM, PLA, PAL)
- VHDL
- Register transfers and Data Paths (registers, buses, ALU, micro-operations, control words)

Other topics such as VHDL programming will also be covered

GRANDE PRAIRIE REGIONAL COLLEGE			
GRADING CONVERSION CHART			
Alpha Grade	**4-point Equivalent**	**Percentage Guidelines**	**Designation**
A^+	**4.0**	**90 – 100**	**EXCELLENT**
A	**4.0**	**85 – 89**	
A^-	**3.7**	**80 – 84**	**FIRST CLASS STANDING**
B^+	**3.3**	**77 – 79**	
B	**3.0**	**73 – 76**	**GOOD**
B^-	**2.7**	**70 – 72**	
C^+	**2.3**	**67 – 69**	**SATISFACTORY**
C	**2.0**	**63 – 66**	
C^-	**1.7**	**60 – 62**	
D^+	**1.3**	**55 – 59**	**MINIMAL PASS**
D	**1.0**	**50 – 54**	
F	**0.0**	**0 – 49**	**FAIL**
WF	**0.0**	**0**	**FAIL, withdrawal after the deadline**

EXAMINATIONS: Midterm Exam; Final Exam and Quizzes

STUDENT RESPONSIBILITIES:

LAB attendance is **mandatory**. You must clear all absences with me; failure to comply will result in a failing grade for the lab component!