Computer Organization and Architecture II
CS 3290

Prerequisite: CS2290 or
Permission of the instructor

Instructor: Libero Ficocelli
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Course Content:

This course will introduce students to the fundamentals of logic design and computer architecture. Important topics will include (but not limited to) basic logic gates and circuits, circuit minimization, combinational logic, sequential logic, latches and flip-flops, registers and register transfers, ALU design, Control unit design, CPU design, I/O operations.

The lectures will stress the theoretical aspects of the material while the labs will deal with actual design and physical construction of digital circuits: we will be using a variety of LSI, MSI, EPROMs, and static rams chips in our circuit construction. We will also be making use of Quartus II software and the Altera UP2 Development kit to implement VHDL programming tasks.

Topics to be covered include:

- Boolean Algebra (basic identities, algebraic manipulation)
- Logic gates
- Cannonical Forms (minterms, maxterms, SOP, POS)
- Applications of Boolean Algebra
- Karnaugh Maps (2,3,4,5 variable maps, implicants prime/essential, covering set)
- Quine-McCluskey Method
- Multiple Output Networks (analysis and design)
- Decoders/Encoders/Priority Encoders (decoder expansion)
- Multiplexers/Demultiplexer (use of MUX in Boolean Function Implementation)
- Latches/Flip-Flops (S-R, D, J-K, Master-Slave, Edge triggered)
- Sequential Circuits (Charactersistic/Excitation Tables, state diagrams, analysis and design)
- Mealy/Moore Machines,
- State Minimization
- Counters (Ripple, Synchronous, Asynchronous, arbitrary, ring)
- Registers (Shift, Bidirectional shift, Parallel load)
- RAM (Static, Dynamic, RAM cells, address decoding, read/write, bit slice model)
- PLDs (ROM, PROM, PLA, PAL)
- VHDL
- Register transfers and Data Paths (registers, buses, ALU, micro-operations, control words)
- Sequencing and Control (CAR, CDR, sequencer, microprograms)

Laboratories:

The Laboratory location for this course is in room E311

Textbook:

Theory: **Digital Electronics with VHDL – *Quartus II Version***
Willian Kleitz

Lab: **Rapid Prototyping of Digital Systems: A tutorial Approach**
Second Edition
James Hamblen and Michael Furman
Copies will be available in the lab

Grading:

Homework Assignments / Lab Assignments/ Lab Reports	30%
Class Quizzes	10%
Midterm	25%
Final Exam	35%

Special Note:

The Student must pass the **theory/concepts** (quizzes, midterm and final exam) portion of the course in order to obtain a passing grade for the term. Failure to achieve a minimum of **50%** on the exam/quiz portion will result in **all** Lab assignments and Homework assignments having a net value of 0.